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Product Code WM-G-MR-09
Product No.

Preliminary Product Specification of WM-G-MR-09

Wireless LAN Module

SOURCE ORGANIZATION: USI WP/RD/WM/HW1

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Date:

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Date:

1 REVISION HISTORY

Version No.	Revised Date	Revised by	Description	Notes
1.0	2007-05-03	Jaddy Chen	Preliminary specification released	
1.1	2007-07-03	Jaddy Chen	Add Recommend Footprint	
1.2	2007-07-04	Jaddy Chen	Revise Pin-out and Footprint	
1.3	2007-07-12	Jaddy Chen	Revise Pin-out pad size	
1.4	2007-07-16	Camus Chen	Revise Supply Voltage, Pin-out and Footprint	
1.5	2007-09-14	Camus Chen	Revise Supply Voltage & Pin Definition	
1.6	2007-09-14	Camus Chen	Revise Supply Voltage & Pin Definition	
1.7	2007-10-12	Camus Chen	Change Module Connection to 36pin LGA	
1.8	2007-12-17	Camus Chen	Revise Mechanical Specification	
1.9	2008-01-10	Camus Chen	Revise Rx Sensitivity , Power Consumption & Mechanical Specification	

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2 PURPOSE

The purpose of this document is to define the product specification for 802.11b/g WiFi module WM-G-MR-09.

3 SCOPE

- High speed for wireless LAN connection: IEEE802.11b/g up to 54Mbps data rate by incorporating Direct Sequence Spread Spectrum (DSSS) and OFDM data modulation.
- Provide seamless roaming within the IEEE 802.11b/g WLAN infrastructure.
- IEEE 802.11b/g compatible: allow inter-operation among multiple vendors.
- Auto fallback: 54M, 48M, 36M, 24M, 18M, 12M, 9M, 6M (802.11g); 11M, 5.5M, 2M, 1M (802.11b) data rate with auto fallback.
- WPA (Wi-Fi Protected Access)
- Support 802.11i Security standard through implementation of AES / CCMP and WEP with TKIP security mechanism.
- Support 802.11e Quality of Service (QoS)
- Interoperability – Complying with WECA WiFi.
- 3-wire, hardware signaling BT WiFi co-existence supported

4 GENERAL FEATURES

	Item	Description	Notes
802.11b/g	Standard	Complies with the latest IEEE802.11b/g wireless LAN Physical Layer Specification (IEEE 802.11g dated 12/6/2003)	
	Chip Set	Marvell 88W8686	
	Module Interface Type	SDIO (1bit and 4 bit) , SDIO_SPI , G-SPI	
	Module Connection	36pin LGA	
	Co-existence	Supports 3-wire BT coexistence scheme for an external BT solution	
	Data Rate	802.11g: 54, 48, 36, 24, 18, 12, 9, 6 Mbps, auto rate 802.11b: 11, 5.5, 2, 1Mbps, auto rate	
	Modulation	OFDM (54, 48, 36, 24, 18, 12, 9, 6Mbps) CCK (11Mbps, 5.5Mbps) DQPSK (2Mbps) DBPSK (1Mbps)	
	Operating Frequency	2.4GHz ISM band	
	Operating Channels	IEEE Channels 1–14 depending on Regulatory Domain settings	
	Others	Compliance with FCC Class B Part 15.247, R&TTE, TELEC major RF regulatory requirements	

5 ELECTRICAL SPECIFICATION

5.1 SUPPLY VOLTAGE

Symbol	Parameter	Min	Typ	Max	Unit
VDD_33	TR SW, ANT SW, PA PE	3.0	3.3	3.6	V
VDD_SHI	Host IF, GPIO, RESETn, CLK_OUT, TMS2	1.62	1.8	1.98	V
		2.97	3.3	3.63	V

5.2 RECOMMENDED OPERATION CONDITIONS

5.2.1 TEMPERATURE, HUMIDITY

Symbol	Parameter	Min	Typ	Max	Unit
TA	Ambient Operation Temperature	-10	-	65	⁰ C
Humidity	Relative Humidity			95	%

Symbol	Parameter	Min	Typ	Max	Units
VDD_33	Power supply voltage with respect to GND	3.0	3.3	3.6	V
VDD_SHI	Power supply voltage with respect to GND	1.62	1.8	1.98	V
		2.97	3.3	3.63	

5.2.2 (SDIO/SPI/JTAG/RESET/COEXISTENCE/GPIO)

DC Electricals.1.8V/3.3V (VDD_SHI/VIO_X2) (VIO_X2 not support 1.8V Mode)

Symbol	Parameter	Operating Mode	Condition	Min	Typ	Max	Units
V18	Power supply voltage	1.8V	--	1.62	1.8	1.98	V
V33	Power supply voltage	3.3V	--	2.97	3.3	3.63	V
VIH	Input high voltage	1.8V	--	1.2	--	V18+0.3	V
		3.3V	--	2.0	--	V33+0.3	V
VIL	Input low voltage	1.8V	--	-0.3	--	0.6	V
		3.3V	--	-0.3	--	1	V
VHYS	Input hysteresis	1.8V	--	250	--	--	mV
		3.3V	--	300	--	--	mV
VOH	Output high voltage	1.8V	--	1.22	--	--	V
		3.3V	--	2.57	--	--	V
VOL	Output low voltage	1.8V	--	--	--	0.4	V
		3.3V	--	--	--	0.4	V
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=3	7.5	12	16	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=3	8	16.5	23	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=3	10	16	22	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=3	10	22	32	mA
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=2	7.5	12	16	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=2	5	11	15.5	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=2	10	16	22	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=2	6.5	14.5	21	mA
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=1	2.5	4	5	mA

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IOL @ 0.4V	Output low current	1.8V	SR[1:0]=1	2.5	5.5	7.5	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=1	3	5	7	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=1	3	7	10.5	mA
IOH @ 1.62V-0.4V	Output high current	1.8V	SR[1:0]=0	2.5	4	5	mA
IOL @ 0.4V	Output low current	1.8V	SR[1:0]=0	2.5	5.5	7.5	mA
IOH @ 1.62V-0.6V	Output high current	1.8V	SR[1:0]=0	3	5	7	mA
IOL @ 0.6V	Output low current	1.8V	SR[1:0]=0	3	7	10.5	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=3	9.5	13.5	16.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=3	10	18	23.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=3	13	18.5	23	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=3	13.5	24.5	33	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=2	9.5	13.5	16.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=2	6.5	12	15.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=2	13	18.5	23	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=2	9	16	22	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=1	3	4.5	5.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=1	3	6	7.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=1	4	6	7.5	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=1	4.5	8	10.5	mA
IOH @ 2.97V-0.4V	Output high current	3.3V	SR[1:0]=0	3	4.5	5.5	mA
IOL @ 0.4V	Output low current	3.3V	SR[1:0]=0	3	6	7.5	mA
IOH @ 2.97V-0.6V	Output high current	3.3V	SR[1:0]=0	4	6	7.5	mA
IOL @ 0.6V	Output low current	3.3V	SR[1:0]=0	4.5	8	10.5	mA
I_pullup	--	--	--	15.7	21.7	28.7	μA
I_pulldown	--	--	--	11.8	22.5	33.1	μA
I_pullup_weak	--	--	--	2.1	2.4	3.4	μA
I_pulldown_weak	--	--	--	1.3	3	4.9	μA

5.2.3 AC ELECTRICAL

Symbol	Parameter	Operating Mode	Condition	Min	Typ	Max	Units
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR ¹ [1:0] = 3	1.8V	0.2*V18 - 0.8*V18	0.58	1.05	1.65	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.81	1.39	2.08	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 3	1.8V	0.8*V18 - 0.2*V18	0.6	1.34	2.38	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.73	1.49	2.21	V/ns
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 2	1.8V	0.2*V18 - 0.8*V18	0.58	1.05	1.65	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.81	1.39	2.08	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 2	1.8V	0.8*V18 - 0.2*V18	0.4	0.88	1.38	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.64	1.29	1.86	V/ns
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 1	1.8V	0.2*V18 - 0.8*V18	0.19	0.34	0.5	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.38	0.59	0.82	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 1	1.8V	0.8*V18 - 0.2*V18	0.2	0.45	0.68	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.36	0.7	0.89	V/ns
T _{SLEW_RISE} @ 10 pF Load	Output rise slew rate when SR[1:0] = 0	1.8V	0.2*V18 - 0.8*V18	0.19	0.34	0.5	V/ns
		3.3V	0.2*V33 - 0.8*V33	0.38	0.59	0.82	V/ns
T _{SLEW_FALL} @ 10 pF Load	Output fall slew rate when SR[1:0] = 0	1.8V	0.8*V18 - 0.2*V18	0.2	0.45	0.68	V/ns
		3.3V	0.8*V33 - 0.2*V33	0.36	0.7	0.89	V/ns

5.3 POWER CONSUMPTION (SDIO MODE)

The power consumption is typical value measured at 25°C temperature

Voltage : VDD3.3

Operating Voltage	3.0~3.6 Volt	
<i>Current</i>		
Condition	Typical (3.3V, 25 degree C)	Maximum (3.3V, 25 degree C)
Transmit(54Mbps, 12 dBm)	270mA	300mA
Transmit(11Mbps, 14 dBm)	270mA	300mA
Receive(54Mbps, -70 dBm)	180mA	210mA
Receive(11Mbps, -70 dBm)	180mA	210mA
Deep Sleep (Use Labtool command 26 1)	0.5mA	1.0mA

5.4 WIRELESS SPECIFICATIONS

The WM-G-MR-09 module complies with the following features and standards:

Features	Description
WLAN Standards	IEEE 802 Part 11b/g (802.11b/g)
Antenna Port	One antenna port support 802.11b/g
Coexistence	Hardware signaling
Frequency Band	2.400 – 2.484 GHz

5.5 RADIO SPECIFICATIONS

Over full range of values specified in the "Recommended Operation Condition" unless specified otherwise.

Features	Description
Frequency Band	2.4000 – 2.497 GHz (2.4 GHz ISM Band)
Number of selectable Sub channels	14 channels
Modulation	OFDM, DSSS (Direct Sequence Spread Spectrum), DBPSK, DQPSK, CCK , 16QAM, 64QAM
Supported rates	1, 2, 5.5, 11, 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Maximum receive level	- 10dBm (with PER < 8%)
Output Power	14 dBm +2.0 /-1.5 dBm for 1, 2, 5.5, 11Mbps 12 dBm +2.0 /-1.5 dBm for 6 , 9 and > 12Mbps

802.11g EVM Requirement

Item	Data Rate (Mbps)	Relative Constellation Error (dB)	EVM (%RMS)
1	6 (BPSK)	-5	56.2
2	9 (BPSK)	-8	39.8
3	12 (QPSK)	-10	31.6
4	18 (QPSK)	-13	22.4
5	24 (16-QAM)	-16	15.8
6	36 (16-QAM)	-19	11.2
7	48 (64-QAM)	-22	7.9
8	54 (64-QAM)	-25	5.6

802.11b EVM

Item	Data Rate (Mbps)	EVM (%RMS)
1	1 (BPSK)	35%
2	2 (QPSK)	35%
3	5.5 (QPSK)	35%
4	11 (QPSK)	35%

Sensitivity

Receiver Characteristics (3.3V, 25 degree C)	Typical	Maximum	Unit
PER <8%, Rx Sensitivity @ 11 Mbps	-85	-83	dBm
PER <8%, Rx Sensitivity @ 1 Mbps	-91	-89	dBm
PER <10% Rx Sensitivity @ 6 Mbps	-86	-84	dBm
PER <10%, Rx Sensitivity @ 54 Mbps	-70	-68	dBm

6 INTERFACE

6.1 PIN DEFINITION

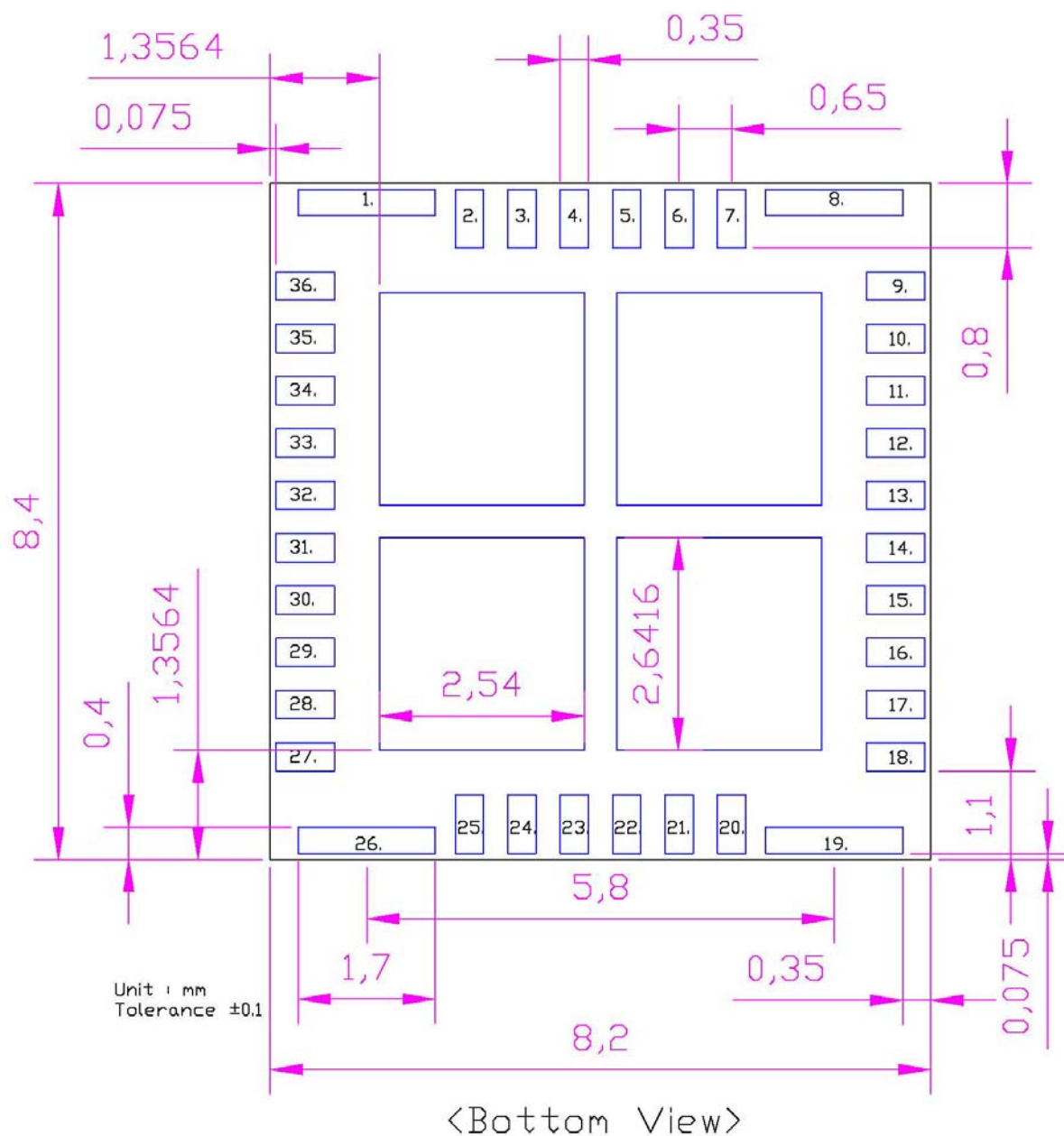
No	Pin Name	Type	Description
1	GND	GND	Ground
2	RF PORT	O	Antenna Port (50ohm)
3	GND	GND	Ground
4	NC	O	NC
5	SD_D1	I/O	SDIO 4-bit Mode: Data Line Bit [1] G-SPI Mode: G-SPI Data Output
6	SCLK	I	NC This is for Boot setting of ROM.
7	ECSn	O	Boot from SPI EEPROM: Pull down by 100kohm Boot from host Interface: NC
8	GND	GND	Ground
9	VDD_SHI	I	Host I/F Voltage: 3.3V Connect to 3.3V power supply Host I/F Voltage: 1.8V Connect to 1.8V power supply Not need to prepare external 1.8V power supply by connecting #9 and #17 (1.8V terminal)
10	GPIO_6	I/O	General I/O Port , leave open if no use.
11	GPIO_5	I/O	General I/O Port , leave open if no use.
12	SD_D3	I/O	SDIO 4-bit Mode: Data Line Bit [3]
13	GPIO_2	I/O	General I/O Port , leave open if no use.
14	SD_CLK	I/O	SDIO 4-bit Mode: Clock Input G-SPI Mode: G-SPI Clock Input
15	GPIO_4	I/O	General I/O Port , leave open if no use.
16	GPIO_1	I/O	General I/O Port t , leave open if no use. Default function : LED indicate.
17	VDD_18	POWER	1.8V DC monitor terminal , need 1uF decoupling capacitor
18	VDD_12	POWER	1.2V DC monitor terminal , need 1uF decoupling capacitor
19	GND	GND	Ground
20	SD_CMD	I/O	SDIO 4-bit Mode: Command / Response G-SPI Mode: G-SPI Data Input
21	SD_D0	I	SDIO 4-bit Mode: Data Line Bit [0] G-SPI Mode: G-SPI Chip Select Input (Active Low)
22	SD_D2	I/O	SDIO 4-bit Mode: Data Line Bit [2] G-SPI Mode: G-SPI Interrupt Output (Active Low)

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23	IF_SEL_1	O	Select Interface Mode Pin SDIO Mode: No Connect G-SPI Mode: Pull Down by 100kohm
24	IF_SEL_2	O	Select Interface Mode Pin SDIO Mode: No Connect G-SPI Mode: Pull Down by 100kohm
25	VDD18A	POWER	1.8V Analog DC monitor terminal , need 1uF decoupling capacitor
26	GND	GND	Ground
27	VDD_33	POWER	Connect to 3.3V DC supply
28	VDD_33	POWER	Connect to 3.3V DC supply
29	BT_STATE	I	Bluetooth State 0 = normal priority, Rx 1 = high priority, Tx Priority is signaled after BT_PRIORITY has been asserted. After priority signaling, BT_STATE indicated the Tx/Rx mode of the BT radio. Please make it open when do not use it.
30	WL_ACTIVE	O	WLAN Active (Active Low) 2-Wire BCA Mode When high, WLAN is transmitting or receiving packets. 3-Wire BCA Mode 0 = Bluetooth device is allowed to transmit 1 = Bluetooth device is not allowed to transmit Internal 50kohm pull-down. This pin drives low when PDn is asserted. In WLAN Sleep mode, all I/O Pads are powered down. This Pad must stay at a low state even in power down mode. Please make it open when do not use it.
31	PDn	I	Pull up by 100kohm, Full Power Down (Active Low)
32	RESETn	I	Reset (Active Low) , leave open if no use.

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33	BT_PRIORITY	I	Bluetooth Priority 2-Wire BCA Mode When high, BT is transmitting or receiving high priority packets. 3-Wire BCA Mode When high, BT is transmitting or receiving packets. Leave open if no use.
34	GPIO_0	I/O	General I/O Port , leave open if no use.
35	SLEEP_CLK	I	Clock Input for External Sleep Clock , leave open if no use.
36	PW_SEL	O	NC



6.2 SPECIFICATIONS AND TIMING DIAGRAM

6.2.1 EXTERNAL SLEEP CLOCK SPECIFICATION

The WM-G-MR-09 external sleep clock pin (SLEEP_CLK) is powered from VDD_SHI

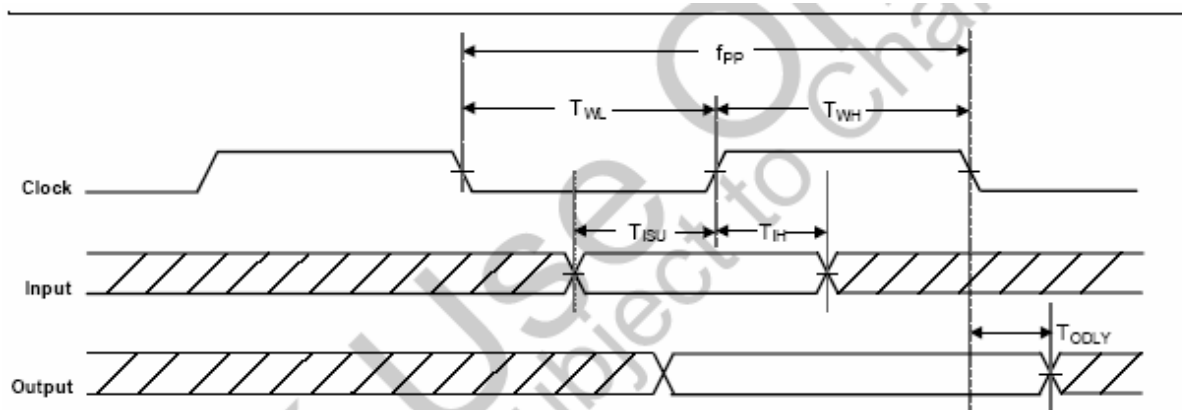
Voltage Supply

Protocol Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
CLK	Clock Frequency Range	--	10	100	1000	kHz
T_{HIGH}	--	--	40	--	--	ns
T_{LOW}	--	--	40	--	--	ns
T_{RISE}	--	--	--	--	5	ns
T_{FALL}	--	--	--	--	5	ns

6.2.2 SDIO PROTOCOL TIMING



Note

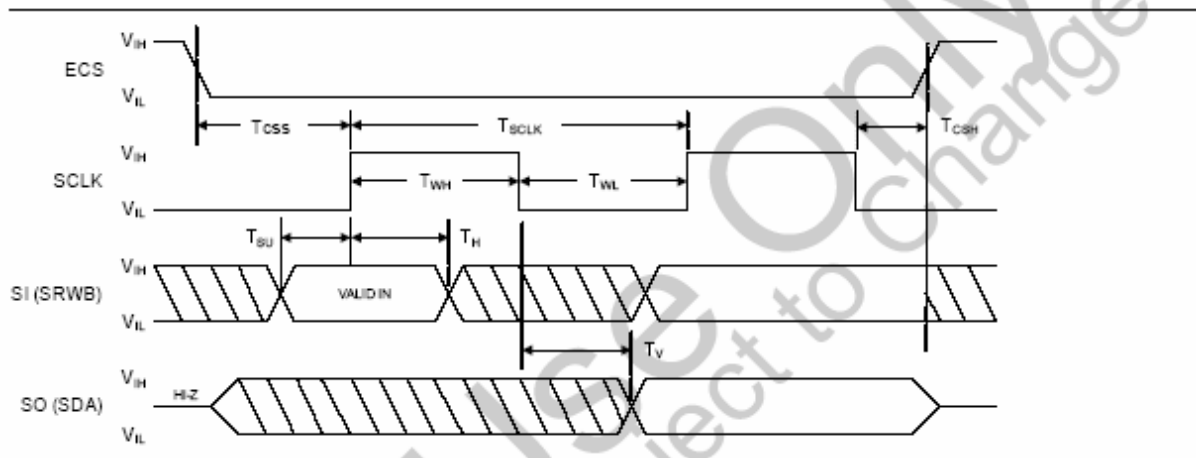
The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

SDIO Timing Data

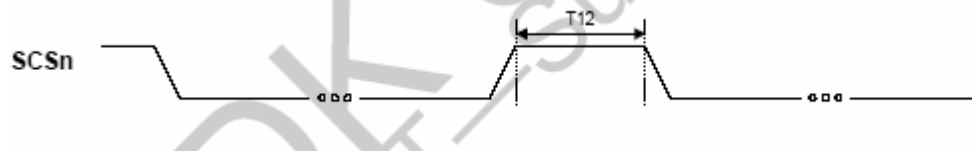
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	CLK Frequency	--	0	--	45	MHz
T_{WL}	CLK Low Time	--	11.1	--	--	ns
T_{WH}	CLK High Time	--	11.1	--	--	ns
T_{ISU}	Input Setup Time	--	5	--	--	ns
T_{IH}	Input Hold Time	--	5	--	--	ns
T_{ODLY}	Output Delay Time	--	0	--	15	ns

6.2.3 SPI PROTOCOL TIMING



G-SPI Interface Inter Transaction Timing



SPI Interface Timing Data

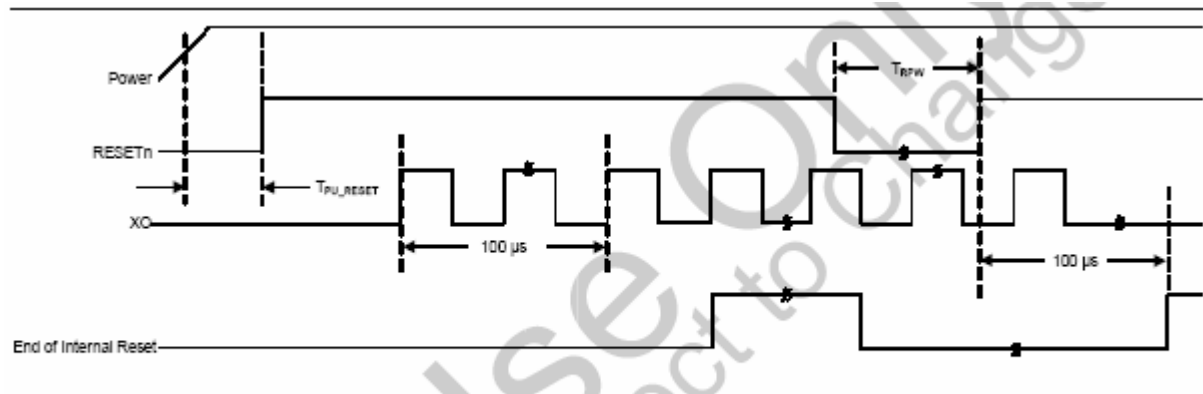
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T1	Clock Period	20	--	--	ns
T2	Clock High	5	--	--	ns
T3	Clock Low	9	--	--	ns
T4	Clock Rise Time	--	--	1	ns
T5	Clock Fall Time	--	--	1	ns
T6	SDI Hold Time	2.5	--	--	ns
T7	SDI Setup Time	2.5	--	--	ns
T8	SDO Hold Time	5	--	--	ns
T9	SDO Setup Time	1	--	--	ns
T10	SCSn Fall to Clock	5	--	--	ns
T11	Clock to SCSn Rise	0	--	--	ns
T12	SCSn Rise to SCSn Fall	400	--	--	ns

6.2.4 CO-EXISTENCE PROTOCOL TIMING

TBD

6.2.5 RESET AND CONFIGURATION TIMING



Notes

- RESETn is not needed for proper operation due to internal power-on reset logic.

RESETn Timing Requirement.

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted	--	0	--	--	ms
T_{RPW}	RESETn pulse width	--	10^1	100	--	ns

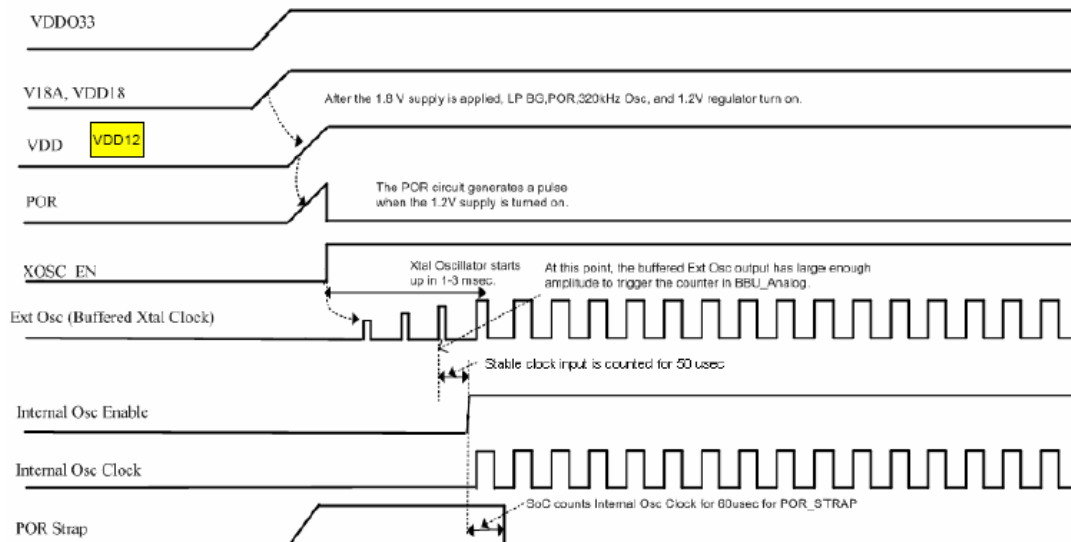
1. This is the minimum value guaranteed for a valid reset. Smaller values may trigger the reset circuit.

Internal Reset Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

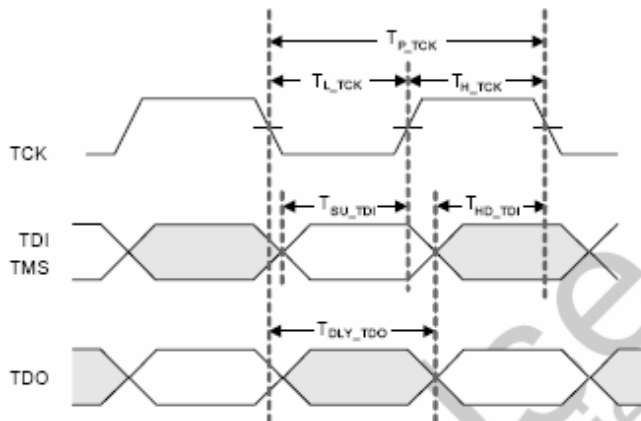
Symbol	Parameter	Condition	Min	Typ	Max	Units
--	Negative internal reset pulse width	--	100	100	--	μ s

6.2.6 POWER UP SEQUENCE



- VDD18 feeds the internal 1.2V regulator (VDD)
- VDD18 must be completely stabilized by 60 us after clock reference stabilizes

6.2.7 JTAG SPECIFICATION



JTAG TIMING

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	--	40	--	--	ns
T_{H_TCK}	TCK High	--	12	--	--	ns
T_{L_TCK}	TCK Low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO Delay	--	0	--	15	ns



Note

Does not apply to CPU JTAG enabled by the TMS_SYS pins.

6.2.8 LED INTERFACE

Pin No.	Pin description	Function description
14	WLAN_LED	Check firmware specification of GPIO(1) with Marvell

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Typ	Units
I _{OH}	Switching current high	Tristate on pad (requires pull-up on board)	Tristate when driving high	mA
I _{OL}	Switching current low	@ 0.4V	10	mA

1. LED Mode is independently selectable for the GPIO[1].

6.2.9 ANTENNA INTERFACE

Antenna diversity is not supported on the Wireless Module.

The output impedance of the antenna port is 50 Ohms.

7 REGULATORY

The WM-G-MR-09 module is tested on module level to comply with following standards (pre-test):

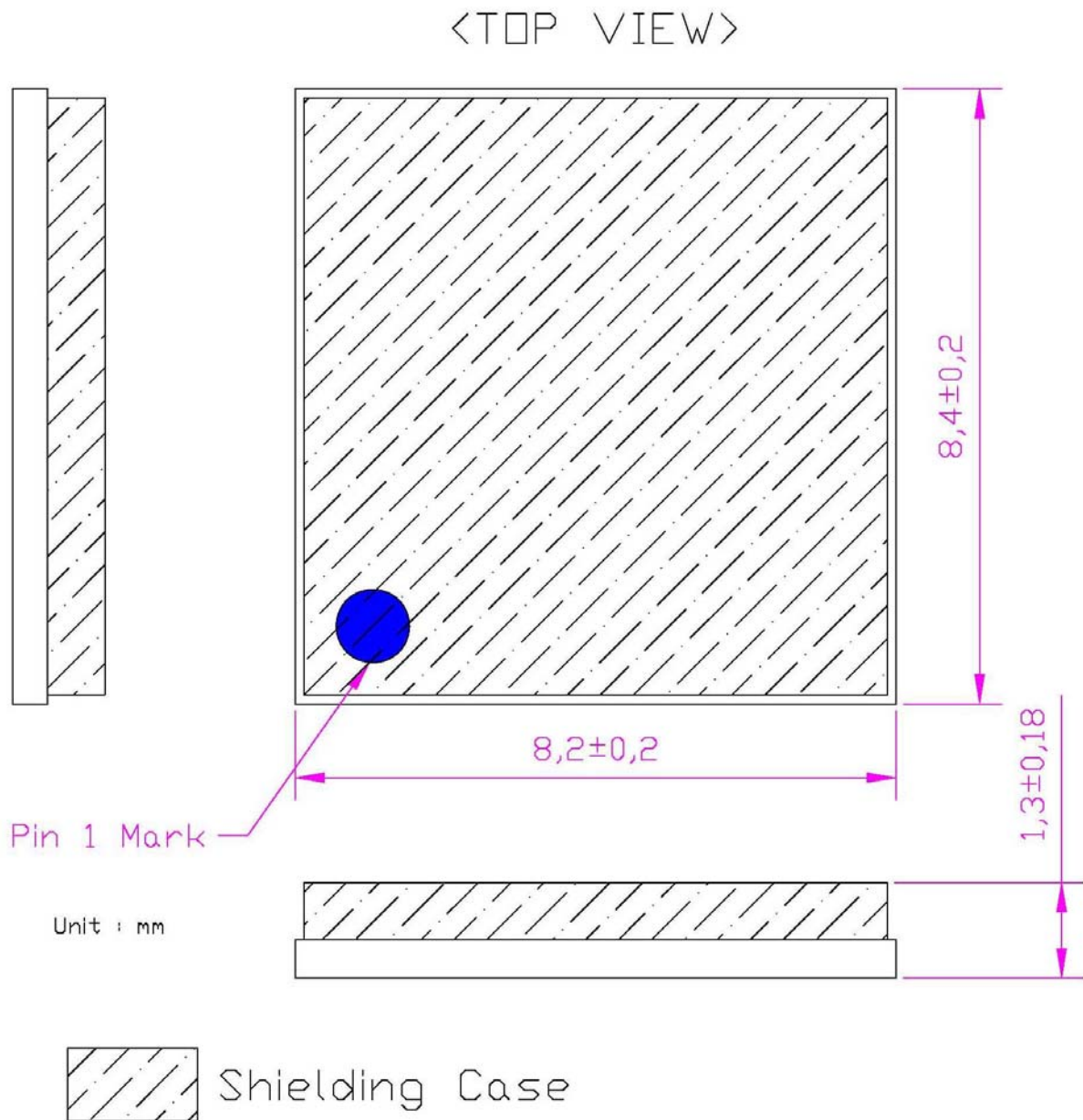
- US/CAN: FCC CFR47 Part 15.247
- Europe: ETS 300-328 V1.6.1

Test setup: laptop plus adaptor card with Marvell Labtool in SDIO mode

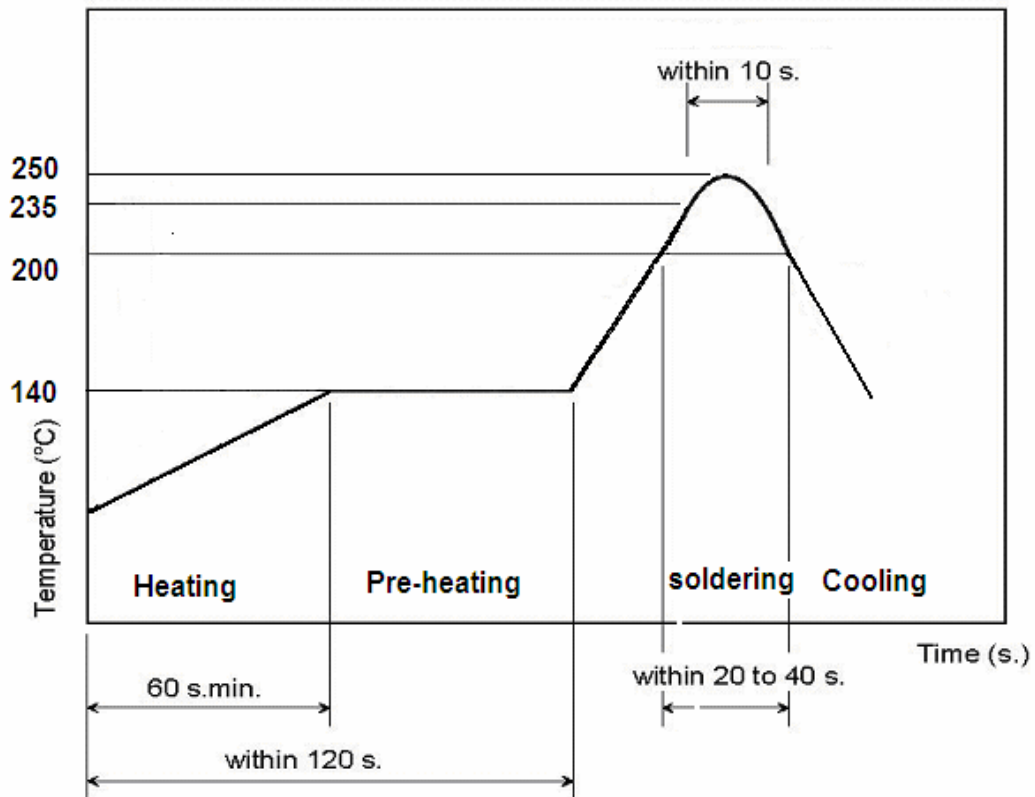
Final certification should be completed on system level.

8 MECHANICAL SPECIFICATION

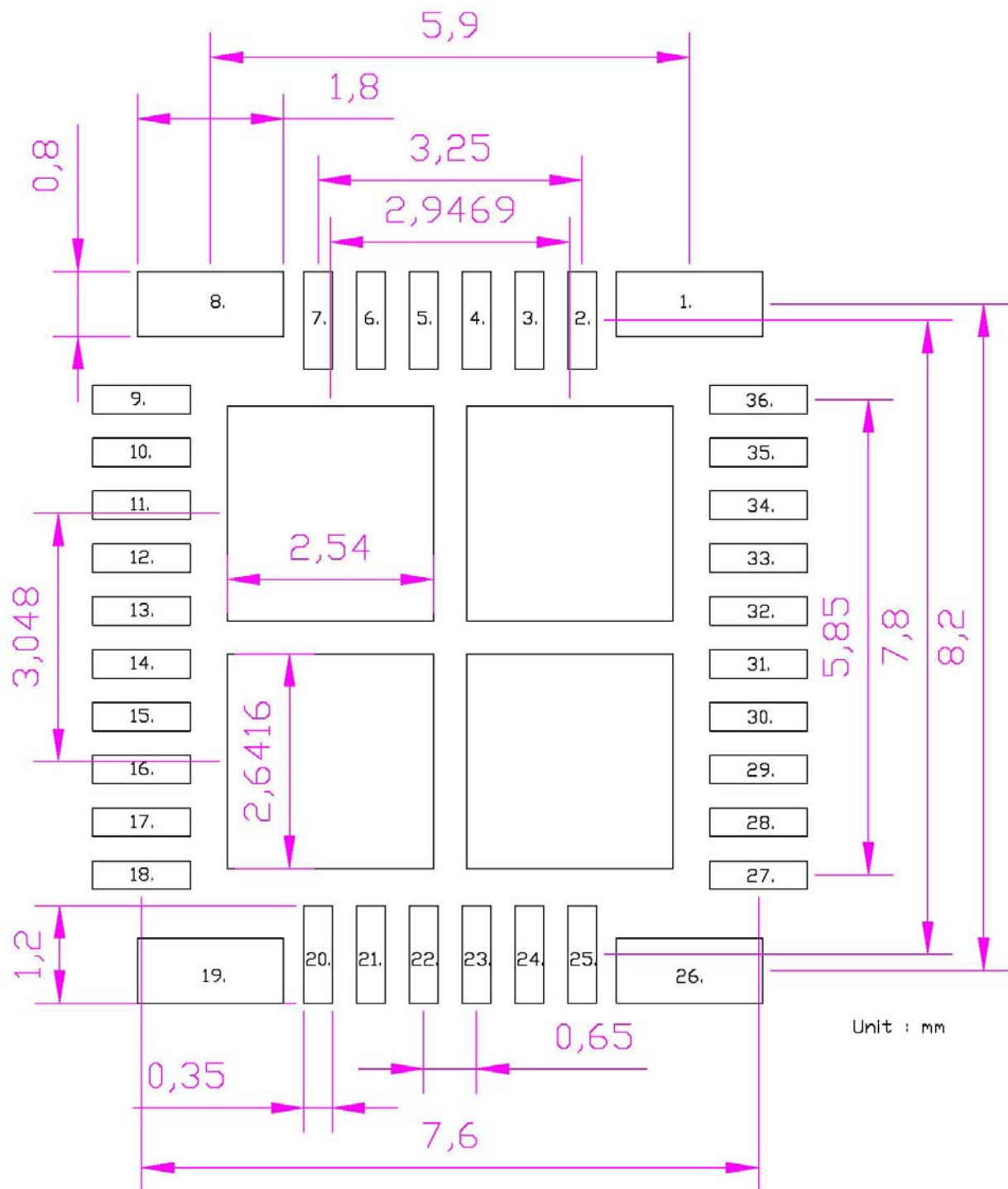
Dimension : 8.2x8.4x1.3 mm



9 RECOMMENDED REFLOW PROFILE



10 RECOMMEND FOOTPRINT



11 PACKAGE AND STORAGE CONDITION

11.1 Package Dimension



11.2 ESD Level

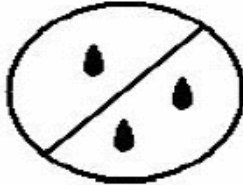
Note:

1. Surface Resistivity:
Interior: $10^9 \sim 10^{11} \Omega/\text{SQUARE}$
EXTERIOR: $10^8 \sim 10^{12} \Omega/\text{SQUARE}$
2. Dimension: 475*420mm
3. Tolerance: +5,0mm
4. Color:
Background : Gray
Text : Red

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11.4 MSL Level / Storage Condition

	<p>CAUTION This bag contains MOISTURE-SENSITIVE DEVICES</p>	<p>LEVEL</p> <div style="border: 2px solid black; padding: 10px; display: inline-block;"> <p style="font-size: 2em; margin: 0;">4</p> </div> <p style="font-size: 0.8em;">If Blank, see adjacent bar code label</p>
<p>1. Calculated Shelf life in sealed bag: 12 months at $< 40^{\circ}\text{C}$ and $< 90\%$Relative humidity (RH)</p> <p>2. Peak package body temperature <u>240</u> $^{\circ}\text{C}$ <small>If Blank, see adjacent bar code label</small></p> <p>3. After bag is opened, Devices that will be subjected to reflow solder or other high temperature process must</p> <p style="margin-left: 20px;">(a) Mounted within: <u>72</u> hrs. Of factory conditions $\leq 30^{\circ}\text{C}/60\%$ RH, OR <small>If Blank, see adjacent bar code label</small></p> <p style="margin-left: 20px;">(b) Stored at $< 10^{\circ}\text{C}$ RH.</p> <p>4. Devices require bake, before mounting, it:</p> <p style="margin-left: 20px;">(a) Humidity indicator Card is $>10\%$ when read at $23\pm 5^{\circ}\text{C}$</p> <p style="margin-left: 20px;">(b) 3a or 3b not met.</p> <p>5. If baking is required, Devices may be baked for 24 hrs at $125\pm 5^{\circ}\text{C}$</p> <p style="margin-left: 20px;">Note: If device containers cannot be subjected to high temperature Or shorter bake times are desired. Reference IPC/JEDEC J-STD-033 for bake procedure</p> <p>Bag Seal Date: _____ Note: Level and body temperature defined by IPC/JEDEC J-STD-020 <small>If Blank, see adjacent bar code label</small></p>		